REMARKS

Claims 1-4, 6-13, 15-21, 24 and 25 were examined and rejected. Applicants amend claims 1 and 20. Applicants submit that no new matter is added therein, as the amendments are supported by claims 8 and 14, Figures 2-4 and paragraphs 15-21 of the application as originally filed. Applicants respectfully request reconsideration of claims 1-4, 6-13, 15-16, 20-22 and 24-25 in view of the following remarks.

I. Claims Rejected Under 35 U.S.C. § 112

The Patent Office rejects claim 15 under 35 U.S.C. § 112, second paragraph, as being indefinite because it recites that identifying occurs after loading which contradicts claim 11. Applicants respectfully disagree as claim 15 requires identifying an additional set of data after loading. Hence, Applicants respectfully request the Patent Office withdraw the rejection above.

II. Claims Rejected Under 35 U.S.C. § 102

The Patent Office rejects claims 1-2 and 6-7 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,119,192 to Kao et al. (Kao). It is axiomatic that to be anticipated every limitation of the claim must be disclosed in a single reference.

Applicants respectfully disagree with the rejection above and submit that claim 1 is patentable over the cited references for at least the reason that the cited references do not disclose a non-volatile memory storing information to load a plurality of configuration registers of a device during a memory design validation test, wherein the non-volatile memory has a maximum memory size less than a memory size sufficient to fill all the configuration registers, as required by claim 1. According to claim 1, for example, the maximum size of the memory is not large enough to store all of the address information and data corresponding to the address information for all of the configuration registers of the device during a memory design validation test. Hence, less than all of the plurality of configuration registers of the device can be loaded using the data in the memory during a memory design validation test.

Kao discloses an interface and memory for providing second initialization parameters from a supplemental parameter memory separate and distinct from the system BIOS memory (see column 2 lines 63-67). Specifically, Kao teaches that "any one or more of the initialization registers can be configured in any desired sequence," (see column 3 lines 13-15) and that the BIOS or supplemental initialization parameters can be used to configure the registers (see column 3 lines 17-20), including a method where a supplemental initialization procedure may be enabled to initialize the controller circuit, or otherwise, if such supplemental initialization procedure is not enabled, initialization of the controller circuit is accomplished using registers from a system BIOS during a normal system boot up routine (see column 3 lines 20-40). Hence, as the Patent Office notes in the final paragraph of page 3 of the current Office Action, the memory has a size equal to a memory size sufficient "to fill some or all of the configuration registers." Thus, since the memory has a size sufficient to fill all of the configuration registers, it does not have a maximum memory size less than a memory size sufficient to fill all of the configuration registers during a memory design validation test, as required by claim 1.

Hence, for at least this first reason, Applicants respectfully request the Patent Office withdraw the rejection above for claim 1.

Now addressing item 14 of the current Office Action where the Patent Office indicated that a memory design validation stage is taught by a configuration mode of Kao because the Applicant has indicated that the memory design validation stage is "only to exclude normal operating mode." Applicant further defines that a memory design validation test or stage, such as claimed, describes a non-volatile memory validation test or stage as known in the art, such as, but not limited to, a stage or test to validate a design of a non-volatile memory, prior to manufacturing of a massive number (e.g., for sale to OEMs and/or the public) of non-volatile memory devices according to the design. Specifically, a memory design validation stage excludes a normal operating mode; as well as any mode of operation of one of a massive number

of manufactured non-volatile memory devices (e.g., devices manufactured according to a validated design, such as for sale to OEMs and/or the public).

Moreove, in some cases, as noted at Figures 2-4 and paragraphs 15-21 of the application as originally filed, a memory design validation stage may include tests in a laboratory, during a design phase of a memory, and/or prior to manufacturing.

On the other hand, Kao, column 2 lines 42-26, descirbes a conventional initialization of a mass manufactured computer system. However, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion in the references of a non-volatile memory storing information to load a plurality of configuration registers of a device during a memory design validation test, as required by claim 1.

Hence, for at least this additional reason, Applicants respectfully request the Patent Office withdraw the rejection above for claim 1.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious for at least the same reasons given above in support of their base claims.

III. Claims Rejected Under 35 U.S.C. § 103

The Patent Office rejects claims 3-4 and 8-10 under 35 U.S.C. § 103(a) as being unpatentable over Kao in view of U.S. Patent Application Serial No. 2004/0143715 to Bonaccio et al. (Bonaccio).

Claim 3 and 4 are submitted as not being anticipated or obvious for at least the same reasons given above in support of their base claims. Hence, Applicants respectfully request the Patent Office withdraw the rejection above for claims 3-4.

Applicants disagree with the rejection above for claim 8 for at least the reason that Kao does not teach repeating during a memory design validation stage as required by claim 8. An argument analogous to the one above for claim 1 and Kao not teaching a memory design validation test, applies here as well.

In addition, Bonaccio fails to cure the shortcomings of Kao. Specifically, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion of repeating during a memory design validation stage in Bonaccio.

Hence, for at least this reason, Applicants respectfully request the Patent Office withdraw the rejection above for claim 8.

The Patent Office rejects claims 11-13, 15-19, 24 and 25 under 35 U.S.C. § 103(a) as being unpatentable over Kao in view of Bonaccio and U.S. Patent No. 6,480,946 to Tomashima et al. (Tomashima). To render a claim obvious, every limitation of that claim must be taught or suggested by at least one properly combined reference.

Applicants respectfully disagree with the rejection above for claim 11 for at least the reason that the cited references do not teach or suggest loading during a memory design validation stage, as required by claim 11. An argument analogous to the one above for claim 8 regarding Kao and Bonaccio not teaching a memory design validation test applies here as well.

In addition, Tomashima fails to cure the shortcomings of the other references. Tomashima teaches reducing skew between read and write signals of a memory system including a plurality of discrete memory devices connected in parallel to a bus to transmit/receive signals to and from a commonly provided controller (see column 1 lines 7-15; column 6 lines 44-53). Also, Tomashima teaches a conventional memory controller performing this reduction by sending a command signal to Vernier circuit 300a during initialization of the memory devices (see column 6 lines 60-65; column 7 lines 30-33) during normal operational mode (see column 37 lines 33-39; column 8 lines 57-62; column 36 line 26 through column 37 line30; and column 38 lines 1-4). However, the initialization stages and operation of conventional memory systems of Tomashima do not describe a memory design validation stage, such as a stage to validate a design of a memory prior to manufacture of memory devices according to that design.

Consequently, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion in the references of loading registers according to test information during a memory design validation stage, as required by claim 11.

Hence, Applicants respectfully request the Patent Office withdraw the rejection above of claim 11.

In addition to the reasons above, Applicants submit that the motivation for combining Tomashima with Bonaccio or Kao is improper. Specifically, Bonaccio and Kao teach programming configuration registers using configuration sets stored in BIOS. On the other hand Tomashima teaches adjusting reference voltage Vref of a Vernier circuit to reduce skew between read and write signals to and from discrete memory devices of a memory system (see Figures 43 and 46; and column 35 line 28 through column 37 line 55). Specifically, Vref is updated using tap circuit 300a which includes a shift register circuit 315, gates, latches and switches (see column 38) which may be initialized by a command applied from the memory controller (see column 37 lines 1-10). Thus, there is no motivation or suggestion in Tomashima for resetting configuration registers and loading configuration registers using information stored in a nonvolatile memory. Consequently, the motivation for such a combination can be gleaned only from Applicants' specification. Hence, the combination is improper. Therefore, for at least this additional reason, Applicants respectfully request the Patent Office withdraw the rejection above.

Any dependent claims not mentioned above are submitted as not being anticipated or obvious for at least the same reasons given above in support of their base claims.

The Patent Office rejects claims 20 and 21 under 35 U.S.C. § 103(a) as being unpatentable over Kao in view of Bonaccio and U.S. Patent No. 5,737,524 to Cohen et al. (Cohen).

Applicants respectfully disagree with the rejection above for at least the reason that the cited references do not teach or suggest a block of control logic adapted to write the plurality of data to the plurality of configuration registers according to the plurality of address information during a memory design validation test, as required by independent claim 20.

An argument analogous to the one above with respect to claim 8 regarding Kao and Bonaccio not teaching a memory design validation test applies here as well.

Also, Cohen teaches loading configuration registers with information which is stored in a non-volatile storage (see column 2 lines 59-64). However, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion in Cohen of the above noted memory design validation test limitation of claim 20.

Thus, none of Kao, Bonaccio, Cohen or their combination teaches or suggests the above noted limitation of claim 20.

Hence, Applicants respectfully request the Patent Office withdraw the rejection above.

CONCLUSION

In view of the foregoing, it is believed that all claims now are now in condition for allowance and such action is earnestly solicited at the earliest possible date. If there are any additional fees due in connection with the filing of this response, please charge those fees to our Deposit Account No. 02-2666.

Respectfully submitted,

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Amber D. Saunders 4/3/07

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